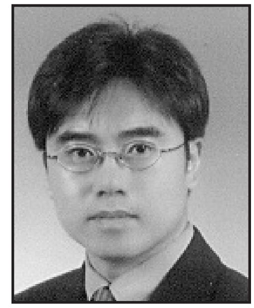
Session 2 Overview

Optical Communications



Chair: *Sung Min Park, Ewha Womans University, Seoul, Korea*

Associate Chair: *Yuriy Greshishchev, Nortel, Ottawa, Canada*

Competitive future of optical communications entirely depends upon the development of low-cost optoelectronic solutions and low-cost high-performance clocking systems. One of the promising and effective ways to reduce cost is the integration of electronics and optical devices in a single chip. Paper 2.1 from Luxtera describes an integrated solution based upon recent advances in SOI photonics. Last year, an optical modulator and a WDM MUX/DEMUX were introduced by the same authors. This year, they introduced an optical interleaver that allows the integration of 4-channel optoelectronic devices. This dramatically reduces the cost of optoelectronics for DWDM applications. Paper 2.9 from Silicon Lab describes a fractional-N PLL in 0.13μm CMOS. It offers a low-cost solution for SONET clock generation with 0.3ps dynamic jitter in OC-192 band. The PLL uses a low-frequency crystal oscillator and a DSP-based loop filter and hence, it does not require any expensive VCXO.

Another way of reducing cost is the use of arrays of VCSEL optical devices. Paper 2.2 from Stanford and Columbia U introduces an optical transceiver exploiting a 4-tap FIR filter transmitter and an integrating/double-sampling receiver in order to remove the front-end transimpedance amplifier (TIA). Compared to Paper 2.1, this work implemented in 90nm CMOS includes a SERDES function with 5:1 MUX/DEMUX ratio.

PON systems currently operate at 1.25Gb/s. The frontier research presented in this session goes far beyond this speed and provides a potential solution even for 20Gb/s and 33.8Gb/s. The areas of interest are burst-mode fast-acquisition CDR circuits and also front-end transimpedance and limiting amplifiers.

Papers 2.3 and 2.4, both from National Taiwan U, describe burst-mode CDRs in 90nm CMOS. The former, based upon injection-locking scheme, operates at 20Gb/s with the acquisition time of 1UI. It also employs 2 gated-VCOs in series for improved jitter performance. The latter introduces a 33.8Gb/s burst-mode CDR, exploiting a new LC gated VCO, a phase selector, and transformer-based circuit solutions to improve input matching and bandwidth.

The next three presentations demonstrate the design of high-performance TIAs. Paper 2.5 from ETRI and ICU describes a burst-mode TIA in 0.18μm CMOS. It incorporates selective internal reset to simplify the burst-mode receiver design for 1.25Gb/s EPON systems. A 3Gb/s TIA is described in Paper 2.6 from National Chiao-Tung U and ITRI, focusing on the bandwidth and gain improvement with the combination of the self-compensated topology with the negative-impedance compensation technique. Paper 2.7 from National Taiwan U and NTU introduces a 40Gb/s transimpedance-AGC amplifier in 90nm CMOS, exploiting reversed triple-resonance networks and negative feedback in a common-gate configuration.

The authors of Paper 2.8 from Yonsei U and Ewha Womans U present a 2.5Gb/s limiting amplifier in 0.18μm CMOS, which employs the negative-impedance compensation technique for gain and bandwidth improvement. Operating with 1.2V power supply, it demonstrates 5.2mW power dissipation.

2.1 A Fully Integrated 4×10Gb/s DWDM Optoelectronic Transceiver in a Standard 0.13µm CMOS SOI 1:30 PM

A. Narasimha, Luxtera, Carlsbad, CA

A 4-wavelength DWDM optoelectronic transceiver, implemented in a 0.13µm CMOS SOI process, achieves an aggregate rate of 40Gb/s transmission over single fiber. The four channel WDM chip, operating all four Txs and Rxs in WDM configuration consumes ~3.5W. This is at nominal operating conditions.

2.2 A 90nm CMOS 16Gb/s Transceiver for Optical Interconnects 2:00 PM

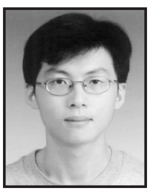
S. Palermo, Stanford University, Stanford, CA,

An optical interconnect transceiver incorporates a 4-tap FIR TX to reduce VCSEL average current and an integrating/double-sampling RX to eliminate the need for a bit-rate TIA. A dual-loop CDR with baud-rate phase detection further reduces power and area. Fabricated in a 1V 90nm CMOS process, the transceiver achieves 16Gb/s operation while consuming 129mW and occupying 0.105mm^2.

2.3 A 20Gb/s Burst-Mode CDR Using Injection-Locking Technique 2:30 PM

J. Lee, National Taiwan University, Taipei, Taiwan

The design and experimental verification of a 20Gb/s CDR circuit based on injection-locking technique is presented. Fabricated in 90nm CMOS technology, this circuit achieves a BER of <10^{-9} for both continuous and burst modes. It has tunability of over 800Mb/s while consuming 175mW. The re-acquisition time of this CDR is 1b interval.



2.4 A 33.6-to-33.8Gb/s Burst-Mode CDR in 90nm CMOS 3:15 PM

L-C. Cho, National Taiwan University, Taipei, Taiwan

A 33.6-to-33.8Gb/s burst-mode CDR circuit is realized in 90nm CMOS technology. The LC gated VCO, the phase selector, the input matching circuit, and the wideband data buffer are discussed. With 2^{11}-1 PRBS input, the measured rms jitter for the recovered data is 1.15ps at 33.72Gb/s. This CDR can tolerate 31 consecutive identical bits with a locking time of 0.2ns(<7b interval). It consumes 73mW from a 1.2V supply excluding the buffers.

2.5 A CMOS Burst-Mode TIA with Step AGC and Selective Internally Created Reset for 1.25Gb/s EPON 3:45 PM

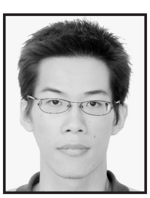
Q. Le, Information and Communcations University, Daejeon, Korea

A selective internal reset mechanism that allows the burst-mode TIA to recover a burst-mode signal as a stand-alone device in EPON is discussed. Using step AGC, the TIA achieves a DR of 27dB and a sensitivity of -31dBm with a PIN photodiode. Moreover, with internal reset, the loud/soft ratio is also 27dB within 100ns guard and preamble times.

2.6 A 40mW 3.5kΩ 3Gb/s CMOS Differential Transimpedance Amplifier Using Negative-Impedance Compensation 4:00 PM

C-M. Tsai, National Chiao Tung University, Hsinchu, Taiwan

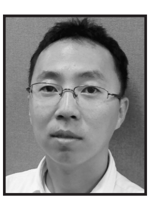
Combining the self-compensated topology with the negative-impedance-compensation technique, a differential TIA with enlarged input-capacitance tolerances is designed in a 0.18µm CMOS technology. The DR is measured to be >20dB without using any gain control. The complete TIA IC consumes 40mW from a 1.8V supply.



2.7 A 40Gb/s Transimpedance-AGC Amplifier with 19dB DR in 90nm CMOS 4:15 PM

C-F. Liao, National Taiwan University, Taipei, Taiwan

A 40Gb/s transimpedance-AGC amplifier is implemented in 90nm CMOS. The TIA uses reversed triple-resonance networks and negative feedback in a common-gate configuration. Operating at 40Gb/s, the amplifier provides 520mV$_{pp}$-diff output swing for a current range of 0.44 to 4mA$_{pp}$, achieved by AGC. The integrated input-referred noise is 3.6µA$_{rms}$ and the total power consumption is 75mW.



2.8 A 1.2V 5.2mW 40dB 2.5Gb/s Limiting Amplifier in 0.18µm CMOS Using Negative-Impedance Compensation 4:30 PM

K. Yoo, Yonsei University, Seoul, Korea,

A 2.5Gb/s limiting amplifier is realized in a standard 0.18µm CMOS process, exploiting the negative-impedance compensation technique. Measurements show 2.5Gb/s operation (0.5pF ESD protection diodes included) with 40dB gain, 21ps$_{rms}$ jitter for 2^{31}-1 PRBS, 9.5mV$_{pp}$ input sensitivity with BER <10^{-12}, and 5.2mW power dissipation from a 1.2V supply. The chip core occupies 0.25×0.1mm^2.

2.9 A Fractional-N PLL for SONET-Quality Clock-Synthesis Applications 4:45 PM

A. Thomsen, Silicon Laboratories, Austin, TX,

A frequency-synthesis IC, targeted toward replacing high frequency XOs and VCXOs, is proposed. It is based on a fixed-frequency XO and a fractional-N PLL. A linearized phase detector, phase-error cancellation, and an integrated shielded LC-VCO are used. The measured jitter is 0.3ps$_{rms}$ in the OC-192 band. The chip draws 70mA excluding the output driver.